Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**Vin**

**GND**

**Vout ( sense)**

**Vout**

**F77T**

**DIE ID**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .0055” X .0055”**

**Backside Potential: GND (or leave floating)**

**Mask Ref: F77T**

**APPROVED BY: DK DIE SIZE .056” X .083” DATE: 9/23/21**

**MFG: ON SEMI THICKNESS .014” P/N: MCC7812AC**

**DG 10.1.2**

#### Rev B, 7/19/02